Amendments to the Specification:

Please replace paragraph 17 with the following amended paragraph:

According to the present invention, techniques for processing for the manufacture of semiconductor devices are provided. But it would be recognized that the invention has a much broader range of applicability. More particularly, the invention provides a method for monitoring a rapid thermal anneal low energy dose implantation process at low temperatures for the manufacture of integrated circuits. For example, the invention can be applied to a variety of devices such as static random access memory devices (SRAM), application specific integrated circuit devices (ASIC), microprocessors and micro controllers, Flash memory devices, and others.

Please replace paragraph 18 with the following amended paragraph:

A method for fabricating a monitor substrate for temperature analysis to monitor a low energy dose implantation process according to an embodiment of the present invention is provided as follows:

Please replace paragraph 28 with the following amended paragraph:

The above sequence of steps is used to prepare a monitor wafer. which will be used to determine an accurate temperature of a rapid thermal anneal process. The monitor wafer is used to make a calibration curve, which will be used to determine a dose of an impurity for another monitor water. The calibration curve can be adjusted depending upon the embodiment. Further details of the present method can be found according to the Figures below.

Please replace paragraph 45 with the following amended paragraph:

Figures 1 through 6 are simplified cross-sectional view diagrams illustrating a method 100 according to an embodiment of the present invention. These diagrams are merely an illustration, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. As shown, the

Appl. No. 10/773,728 Amdt. dated April 26, 2005 Reply to Office Action of February 24, 2005

method 100 begins by providing a monitor substrate 101, which can be a silicon wafer or the like. Alternative substrates can include any suitable material such as boron epitaxial silicon and silicon on insulator substrate. Preferably, the monitor wafer is the silicon wafer.

Please replace paragraph 47 with the following amended paragraph:

Next, the method provides a method of introducing introduces a dopant impurity 305 at low energy and high dose into a depth of the monitor wafer. The dopant impurity can be a boron bearing species, an arsenic bearing species, and others. The energy is often 2 KeV to less than 2 KeV, but can also be at others. The dose is 4 x 10 ¹⁴ to 1 x 10 ¹⁵ atoms/cm², but can also be others. Preferably, the method is used for low energy high dose impurities for shallow junction devices. These devices often have junction depths of less than 40 nm, but can also be at other depths. Additionally, the shallow junction devices are often for line rules of less than 0.15 um. Of course, the particular energies, doses, and depths depend upon the application.

Please replace paragraph 62 with the following amended paragraph:

Referring to Figure 7, we plotted Rs-to-dose sensitivity testing results. The implantation conditions included $\frac{10^{15} \text{ silicon/20 KeV/1 x } 10^{15} \text{ atoms/cm}^2 \text{ before boron/2 KeV/4 x } 10^{14} \text{ atoms/cm}^2 \text{ silicon/20 KeV/1 x } 10^{15} \text{ atoms/cm}^2 \text{ before boron/2 KeV/4 x } 10^{14} \text{ atoms/cm}^2$. Annealing conditions included 700°C, 30 seconds, $N^2 N_2$ as annealing ambient. Referring to Figure 8, we have demonstrated the dependence of Rs changes upon annealing temperature. Here, implantation conditions included silicon/20 KeV/1 x 10^{15} atoms/cm² before boron/2 KeV/4 x 10^{14} atoms/cm² and annealing conditions used were from 650 to 700°C, 30 seconds, $N^2 N_2$ as annealing ambient.